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# ACTIVE MATRIX SUBSTRATE, PRODUCTION METHOD OF ACTIVE MATRIX SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE AND ELECTRONIC EQUIPMENT

[Akutibu matorikusu kiban, akutibu matorikusu kiban no seizo hoho, ekisho hyoji sochi, oyobi denshi kiki]

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SPECIFICATION /1*

# ACTIVE MATRIX SUBSTRATE, PRODUCTION METHOD OF ACTIVE MATRIX SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE AND ELECTRONIC EQUIPMENT

## INDUSTRIAL FIELD

The present invention pertains to an active matrix substrate applied, for example, to an active matrix liquid crystal display, and production methods thereof. The present invention also pertains to a liquid crystal display device and electronic equipment applying these production methods. More particularly, the present invention pertains to an annealing treatment for melt-crystalizing a semiconductor film on the surface of a substrate.

## PRIOR ART

Semiconductor films such as polycrystalline silicon are widely used in thin film transistors (hereafter called TFT in this specification) and solar cells. These semiconductor devices depend strongly for their performance on the quality of the semiconductor film comprising the performing parts of these semiconductor devices. Needless to say, obtaining high quality semiconductor films gives semiconductor devices of correspondingly high performance. For example, polycrystalline silicon (poly-Si) of higher film quality gives TFT with better high-speed switching operation by polycrystalline silicon thin film transistors (poly-Si TFT) used, for example, in liquid crystal display devices. Semiconductor films with high crystallization efficiency must have a great difference in light absorption efficiency to give high energy conversion efficiency when used in solar cells. There is a strong demand for crystalline semiconductor films of such high quality.

However, such high-quality semiconductor films are usually difficult to form and subject to great restrictions. Polycrystalline silicon films have been formed in the TFT field with relatively high mobility by fabricating transistors at a high treatment temperature, where the maximum treatment temperature is about 1000°C. As a result, the substrates on which semiconductor films or semiconductor devices can be fabricated are limited to substrates which have enough heat resistance to withstand a high-temperature heat treatment. Previous poly-Si TFT, therefore, have been fabricated on small quartz glass substrates, all of which are expensive. Solar cells usually use

*Numbers in the margin indicate pagination in the foreign text.

amorphous silicon (a-Si) for the same reason.

Thin film transistors (hereafter called TFT) in active matrix substrates of liquid crystal display devices are preferably produced by a low-temperature treatment allowing an inexpensive glass substrate to be used for the substrate. Of the silicon films required to form, for example, the channel areas of these TFT, amorphous silicon films can be formed by a low-temperature treatment, but have the drawback of low TFT mobility. /2

Therefore, a method has been proposed for forming a polysilicon TFT with high mobility by subjecting an amorphous silicon film formed on a glass substrate to laser crystallization by irradiating a laser beam to melt-crystallize the amorphous silicon film while moving the substrate. The usual method adopted is to fabricate a polysilicon film of large area by moving the substrate relative to the laser beam while overlapping pulse lasers. This can improve TFT mobility by at least a factor of ten compared to amorphous silicon.

Laser crystallization by irradiating a laser while moving a substrate as in prior art, however, has the problem of causing uneven polysilicon film due to deviations between the laser oscillating pulses and overlapping laser irradiation areas. It also has the problem that it cannot fabricate polysilicon film of good quality unless a laser is irradiated at least ten times in the same location, and as a result, cannot achieve improved throughput.

Reflecting on these problems, the purpose of the present invention is to provide an active matrix substrate and production methods thereof which can produce even laser crystallization on semiconductor films formed on a substrate, and achieve high throughput.

## DISCLOSURE OF THE INVENTION

To solve these problems, the present invention is a production method for an active matrix substrate having a plurality of scanning lines and a plurality of data lines extending perpendicular to each other in the planar directions on the substrate, and pixel electrodes and pixel thin film transistors formed opposite each other in a plurality of pixel areas partitioned by said data lines and said scanning lines, characterized by applying a laser annealing treatment for irradiating a semiconductor film for forming said pixel thin film transistors on the surface of said substrate by a line beam having laser beam irradiation areas elongated in an X direction and a half width in a laser beam intensity profile in an Y direction narrower than the pixel spacing in the Y direction, where the direction in

which said pixel thin film transistors are arranged on nearly the same line is the X direction and the direction perpendicular to this is the Y direction, in the annealing treatment for melt-crystallizing said semiconductor film after forming said semiconductor film. /3

Unevenness of laser-crystallized polysilicon film produces a period matching the feed spacing of the substrate during laser irradiation. That is, if the beam width of the laser beam in the scanning direction is narrower than the pixel spacing, scanning irradiation while overlapping this laser will at least prevent an uneven period becoming greater than the pixel spacing. This can greatly reduce polysilicon film unevenness.

In a preferred mode of the present invention, said substrate and said line beam are moved relative to each other in the Y direction to continuously melt-crystallize said semiconductor film during said laser annealing treatment, and said line beam selectively irradiates the areas in the Y direction of said semiconductor film which match the projected formation areas of said pixel thin film transistors. Such a configuration can reduce time spent irradiating the laser on unnecessary areas, which can shorten annealing time while assuring evenness, and improve throughput.

In a preferred mode of the present invention, said substrate and said line beam are moved relative to each other in the Y direction to continuously melt-crystallize said semiconductor film during said laser annealing treatment, and said line beam selectively and repeatedly irradiates the areas in the Y direction of said semiconductor film which match the projected formation areas of said pixel thin film transistors.

In a preferred mode of the present invention, said laser annealing treatment is applied before the patterning step for patterning said semiconductor film. This is so that the laser annealing treatment does not damage an underlayer protective film if an underlayer protective film has been formed on the surface of the substrate.

In this case, the alignment between the anneal pattern during said laser annealing treatment of said semiconductor film and the mask pattern used during said patterning step uses the fact that the hue of said semiconductor film after said laser annealing treatment differs depending on the degree of irradiation of the line beam. Such a configuration directly aligns the mask with the anneal pattern, which can minimize deviations in TFT characteristics and simultaneously improve throughput even more by crystallizing only the channel areas. /4

This alignment between the anneal pattern during said laser annealing treatment of said semiconductor film and the mask pattern used during said patterning step is performed using an alignment mark made in an underlayer protective film formed on the bottom layer side of said semiconductor film.

In a preferred mode of the present invention, said laser annealing treatment may be applied after said patterning step for patterning said semiconductor film.

In a preferred mode of the present invention, coating a photocuring resin on a specific location of said substrate before said laser annealing treatment, and irradiating a laser beam on said photocuring resin during said laser annealing treatment to cure said photocuring resin aligns the mask to be used thereafter with said substrate.

In the present invention, said pixel thin film transistors are formed with the channel length direction in the X direction. Such a configuration inhibits producing a part which does not require annealing in the channel length direction, which stabilizes the electrical characteristics of the TFT. This also has the advantage that the alignment precision in the channel length direction during the patterning step can be relaxed when the patterning step is applied after the laser annealing step.

In a preferred mode of the present invention, when a drive circuit provided with drive circuit thin film transistors has been constituted on said substrate on a Y-direction side of the active matrix part formed in said pixel areas, the projected formation area of said drive circuit is also annealed during said laser annealing treatment. Such a configuration can crystallize the semiconductor film comprising a TFT without skips even without aligning the TFT with the drive circuit.

In this case, the movement speed when moving said substrate and said beam line relative to each other in the Y direction is varied during said laser annealing treatment to selectively anneal a specific area of said semiconductor film.

In an especially preferred mode, the movement speed when moving said substrate and said beam line relative to each other in the Y direction during said laser annealing treatment is lower when irradiating said line beam on the projected formation area of said drive circuit than when irradiating said line beam on the projected formation areas of said pixel thin film transistors.

Such a configuration can increase the movement of the TNG comprising the drive circuit while increasing throughput. /5

In a preferred mode of the present invention, said laser annealing treatment is applied with an optical system having a spot beam for selectively irradiating said line beam on the areas in the X direction of said semiconductor film which match the projected formation areas of said pixel thin film transistors disposed in a location midway on the irradiation path of said laser beam. By disposing an optical system having a spot beam for selectively irradiating said line beam on the areas in the X direction of said semiconductor film which match the projected formation areas of said pixel thin film transistors, such a configuration does not irradiate a laser beam on unnecessary areas in the X direction as well, which allows the intensity of the laser beam on the necessary areas to be increased to that extent.

In a preferred mode of the present invention, said semiconductor film is subjected to rapid thermal annealing in said annealing step after said semiconductor film has been subjected to said laser annealing treatment. Conversely, said semiconductor film may be subjected to said laser annealing treatment after said semiconductor film has been subjected to said rapid thermal annealing.

In this case, the laser for applying said laser annealing treatment is preferably irradiated simultaneously with the light beam for applying rapid thermal annealing to said irradiated substrate.

In a preferred mode of the present invention, the light beam for applying rapid thermal annealing is also irradiated simultaneously during said annealing step on an area containing the area irradiated by the laser beam for applying said laser annealing treatment.

Working examples of the present invention will be discussed referring to the appended drawings.

Configuration of an Active Matrix Substrate

Fig. 1(A) is a schematic diagram illustrating the configuration of an active matrix substrate in a liquid crystal display device.

In this drawing, a liquid crystal display device (1) has a pixel area (5) formed by partitioning by data lines (3) and scanning lines (4), where a liquid crystal capacitor (6) of a liquid crystal cell for inputting image signals is constituted through pixel TFT (10). In the following discussion, the two orthogonal directions on the active matrix substrate (2) are called the X direction and the Y direction, where the scanning lines (4) extend in the X direction and the data

lines (3) extend in the Y direction. Moreover, the X direction is not limited in this specification to the X direction just defined (the direction in which the scanning lines (4) extend), and the Y direction is not limited to the Y direction just defined (the direction in which the data lines (3) extend). The X direction may also in this specification mean the direction in which the data lines (3) extend, and the Y direction may also in this specification mean the direction in which the scanning lines (4) extend. /6

A data driver part (7) for the data lines (3) comprises a shift register (71), a level shifter (72), video lines (73), and analog switches (74). A scan driver part (8) for the scanning lines (4) comprises a shift register (81) and a level shifter (82). A holding capacitor (51) is also formed in the pixel area between the pixel area and the scanning lines of the previous stage.

Although the TFT (10) in the active matrix part comprising the data lines (3), the scanning lines (4), the pixel areas (5), and the TFT (10) are aligned in the X direction and the Y direction, the CMOS circuits or the like comprising N-type TFT n1 and n2 and P-type TFT p1 and p2 are formed at high density in the data driver part (7) as shown by the two stages of invertors in Fig. 1(B). Therefore, the N-type TFT n1 and n2 and P-type TFT p1 and p2 formed in these circuits are not limited to being aligned in the X direction and the Y direction. The TFT (10) in the active matrix part (9), however, have the same fundamental configuration as the N-type TFT n1 and n2 and P-type TFT p1 and p2 in the data driver part (7), and are produced in the same step.

An active matrix substrate (2) may comprise only an active matrix part (9) on a substrate, a data driver part (7) on the same substrate as an active matrix part (9), a scan driver part (8) on the same substrate as an active matrix part (9), or both a data driver part (7) and a scan driver part (8) on the same substrate as an active matrix part (9). A driver housing type active matrix substrate (2) may be a complete driver housing type comprising all of the components contained in a data driver part (7), such as a shift register (71), a level shifter (72), video lines (73), and analog switches (74), on an active matrix substrate (2), or a partial driver housing type comprising some of these components on an active matrix substrate (2). An active matrix substrate (2) can also comprise all of a data driver part (7) or a scan driver part (8) on a substrate, or only part of these on a substrate. The present invention can be applied to any of these types. The example in the following discussion is an active matrix substrate (2) comprising a data driver part (7) on a Y-direction side of an active matrix part (9). Fig. 1(A), moreover, shows a data driver part (7) on only one Y-direction /7

side of an active matrix part (9), but data driver parts (7) are often formed on both Y-direction sides of an active matrix part (9). Therefore, the following discussion will also discuss an example comprising data driver parts (7) formed on both Y-direction sides of an active matrix part (9).

Fig. 2 is an enlarged plan showing one of the pixel areas of a active matrix substrate. Fig. 3(A) is a section of Fig. 2 taken at line I-I', and Fig. 3(B) is a section of Fig. 2 taken at line II-II'. The TFT in the data driver part, which are not shown, have basically the same configuration.

In these drawings, the TFT (10) in each pixel area (5) comprises a source area (11) electrically connected to a data line (3) through a connect hole (17) in an interlayer insulating film (16), a drain area (12) electrically connected to a pixel electrode (19) through a connect hole (18) in the interlayer insulating film (16), a channel area (13) for forming a channel between the drain area (12) and the source area (11), and a gate electrode (15) branching from the channel area (13) through a gate insulating film (14) on a glass substrate (20). This gate electrode (15) comprises part of a scanning line (4). Moreover, an underlayer protective film (21) comprising, for example, a silicon nitride film or a silicon oxide film is formed on the surface of the glass substrate (20).

If formed in the same location between each pair of pixel areas (5), TFT (10) may be formed symmetrically with the adjacent pixel area (5), but TFT (10) often are aligned in one of the X direction or the Y direction. The following production method in this example uses such an alignment configuration.

TFT Production Method

A TFT production method according to Working Example 1 of the present invention will be discussed referring to the drawings.

In this example, the following steps are applied using a 235 mm square non-alkaline glass substrate.

Fig. 4 is a TFT step section corresponding to the section of Fig. 2 taken at line I-I', and Fig. 5 is a TFT step section corresponding to the section of Fig. 2 taken at line II-II'. The TFT in the data driver part are not shown, as they have basically the same configuration. /8

Underlayer Protective Film Formation Step

In Figs. 4(A) and 5(A), if using a silicon oxide film for the

underlayer protective film (21), first, a 500 to 2000 Ångstroms thick silicon oxide film, which will become the underlayer protective film (21), is formed by ECR-PECVD on the surface of the substrate (20) under temperature conditions of 250°C to 300°C. A silicon oxide film can also be formed by APCVD, in which case, the temperature of the substrate (20) is set in a range from 250°C to 450°C and monosilane ($SiH_4$) and oxygen are used as raw material gases to form a silicon oxide film.

Semiconductor Film Deposition Step

Next, an undoped pure silicon film (semiconductor film) (30) is deposited to a thickness of about 200 to 1000 Ångstroms on the surface of the underlayer protective film (21). LPCVD, PECVD, or sputtering may be used when forming a silicon film (30). According to these methods, the film formation temperature can be set in a range up to about 500°C.

Annealing Step

Next, a laser beam irradiates the amorphous silicon film (30) as shown in Figs. 4(B), 5(B), and 5(C) to improve the silicon film (30) to polycrystalline silicon. In this example, a xenon chloride (XeCl) excimer laser (308 nm wavelength) is irradiated (laser annealing treatment: annealing step). The laser is irradiated in this step in a vacuum atmosphere or an inert gas or oxygen atmosphere with the substrate (20) heated to any desired temperature from room temperature to about 500°C.

In the state before this annealing step (the state shown in Figs. 4(A) and 5(A)), an underlayer protective film (21) and a silicon film (30) have been formed over the entire surface of the glass substrate (20) as shown in Fig. 6, but the parts of the silicon film (30) which will become the source area (11), the drain area (12), and the channel area (13) of the TFT (10) in the active matrix part (9) are shown by the dotted lines L1 in Fig. 6, and the parts that will become the source area (11), the drain area (12), and the channel area (13) of the TFT (10) in the data driver part (7) are shown by the dotted lines in Fig. 6.

Therefore, in this example, a laser beam selectively irradiates /9
those areas of the silicon film (30) in the Y direction which match the projected formation areas A1 of the TFT (10) for the active matrix part (9), and the laser beam deliberately does not irradiate the areas B2 between the projected formation areas A1 of the TFT (10).

Although a data driver part (7) likewise provided with TFT (10) is constituted on a Y-direction side of the active matrix part (9) on the substrate (20), unlike the active matrix part (9), the projected formation area of the TFT (10) is usually just a linear array in the X direction as shown by the dotted lines L2 from the standpoint of placing many TFT (10) in a narrow area of this data driver part (7). Therefore, because a laser beam cannot selectively irradiate the projected formation area of the TFT (10) for the data driver part (7), a laser beam irradiates all of the areas A2. The laser beam deliberately does not, however, irradiate the areas B2 between the active matrix part (9) and the data driver part (7).

In this example, a line beam L0 having a laser beam irradiation area L4 extending in the X direction and a half width in a laser beam intensity profile in the Y direction narrower than the pixel spacing in the Y direction (for example, a line beam with a laser pulse repeating frequency of 100 to 1000 Hz, and preferably 200 Hz) irradiates the silicon film (30) as shown in Fig. 7(A). Specifically, a line beam is used in which the half width L21 (the width of the area matching 1/2 the intensity of the peak H) in a laser beam intensity profile, in which the location in the Y direction in the line beam irradiation area L4 is shown on the horizontal axis and the intensity of the laser beam is shown on the vertical axis, is narrower than the pixel spacing PY in the Y direction as shown in Fig. 7(B). Because the output of the laser source is limited, it is important that this beam can be rectified in some way to most efficiently form an even polysilicon film. Therefore, forcibly narrowing the width of the beam in the Y direction and forcibly elongating the width in the X direction in the present invention can assure throughput and improve evenness. The spatial distribution of crystallinity in a laser-crystallized silicon film is dependent on the laser beam intensity profile and the rate of overlap of this line beam L0. If the half width L21 of a laser beam is larger than the pixel spacing PY as in prior art, the period of the crystallinity distribution is always greater than the pixel spacing PY. Using a laser beam with a half width L21 narrower than the pixel spacing PY and irradiating this laser beam while overlapping, by contrast, can /10
control the crystallinity distribution to a period less than the pixel spacing PY. This can greatly reduce deviations in the TFT. Therefore, as shown in Fig. 7(C), the width of the area matching 1/2 the intensity of the peak H is also considered the half width L21 for a laser beam having a laser beam intensity profile which is not a gaussian distribution and a specific width for the area showing the peak H.

When using such a laser beam (line beam L0) to anneal the silicon film (30) in this example, the position of the line beam L0

is fixed and the silicon film (30) is continuously melt-crystallized by moving the substrate (20) by a stage (40) toward the Y direction as shown in Fig. 8(A). During this process, the half width L21 in the laser beam intensity profile in the Y direction in the line beam irradiation area L4 is narrower than the pixel spacing PY. As a result, the line beam L0 deliberately does not irradiate the areas B1 which do not require laser annealing treatment while the line beam L0 irradiates the projected formation areas A1 of the TFT (10).

Therefore, as shown in Fig. 8(B), the stage (40) is moved at low speed when the line beam L0 irradiates the projected formation areas A2 of the data driver part (7), and the stage (40) is moved at high speed when the line beam L0 irradiates the areas B2 between the data driver part (7) and the projected formation areas of the TFT (10). The stage (40) may also be moved at the same speed in both the projected formation areas A2 of the data driver part (7) and the projected formation areas A1 of the TFT (10). The stage (40) is also moved at low speed when the line beam L0 irradiates the projected formation areas A1 of the TFT (10), and the stage (40) is moved at high speed when the line beam L0 irradiates the areas B1 between the projected formation areas A1 of the TFT (10). As a result, the line beam L0 selectively melt-crystallizes an amorphous silicon film (30) to a polycrystalline silicon film in only the areas of the silicon film (30) which are irradiated for a long time.

Annealing in this way selectively and continuously irradiates a line beam L0 on the projected formation areas A2 of the data driver part (7) and the projected formation areas A1 of the TFT (10) in the active matrix part (9), and can therefore raise the throughput while fabricating a high-quality polysilicon film from the silicon film (30) in the projected formation areas A2 of the data driver part (7) and the projected formation areas A1 of the TFT (10) in the active matrix part (9). Because the data driver part (7) especially demands TFT (10) with a faster operating speed, as shown in Fig. 8(B), the stage (40) is moved at as slow a speed as possible when the line beam L0 irradiates the projected formation areas A2 of the data driver part (7), or the number times that the line beam L0 irradiates the projected formation areas A2 of the data driver part (7) is increased. /11

Silicon Mask Patterning Step

Next, after applying the annealing step, the silicon film (30) is patterned using the photolithography technique to produce an island-shaped silicon film (31) as shown in Figs. 4(C), 5(D), and 9. The alignment between the anneal pattern of the laser annealing treatment applied to the silicon film (30) and the mask pattern used

in this patterning step uses the fact that the hue of the silicon film (30) after laser annealing treatment differs depending on the degree of irradiation of the line beam L0. Specifically, the amorphous silicon film (30) is red before irradiating the laser beam L0, and the polycrystalline silicon film (30) produced by irradiating the laser beam L0 is yellow. Therefore, the boundary between red areas and yellow areas is used as a reference to align the anneal pattern on the silicon film (30) with the mask pattern for this patterning. If laser annealing has been applied at the same spacing as the pixel spacing PY in the Y direction, aligning the mask with the anneal pattern for alignment can fabricate pixel TFT with few deviations at a high throughput.

Gate Electrode Film Formation Step

Next, a gate oxide film (14) comprising a 600 to 1200 Ångstroms thick silicon oxide film is formed on the silicon film (31) as shown in Figs. 4(D) and 5(E), for example, by ECR-PECVD under conditions of 250°C to 300°C.

Gate Electrode Formation Step

Next, a 3000 to 6000 Ångstroms thick tantalum thin film is formed by sputtering on the surface of the gate oxide film (14) as shown in Figs. 4(D) and 5(E), then patterned using the photolithography technique to form a gate electrode (15). /12

Impurity Introduction Step

Next, a bucket-type quantitative non-separating ion injector (ion doping device) is used to inject impurity ions into the silicon film (31) using the gate electrode (15) as a mask. This forms a self-aligning source area (11) and drain area (12) on the gate electrode (15). The part of the silicon film (31) not injected with impurity ions during this process becomes the channel area (13). These source and drain areas are a self-aligning type injected with ions using the gate as a mask, but are not limited to this type. Other possibilities are an LDD configuration containing a low concentration in the source and drain areas, or an offset configuration injected with ions using a mask covering the gate electrode.

Diborane ($B_2H_6$) diluted with oxygen gas to a concentration of 5% is used as the raw material gas when forming a P-channel TFT.

Interlayer Insulating Film Formation Step

Next, a silicon oxide film with a thickness of 5000 Ångstroms is formed as an interlayer insulating film (16) as shown in Figs. 4(E)

and 5(F) by PECVD under temperature conditions of 250°C to 300°C.

Activation Step

Next, the injected ions are activated and the interlayer insulating film (16) is improved by heat-treating in a 300°C oxygen atmosphere for one hour.

Metallizing Step

Next, contact holes (17) and (18) are formed in the interlayer insulating film (16). Later, a source electrode (data line (3)) is electrically connected to the source area (11) and a drain electrode (pixel electrode (19)) is electrically connected to the drain area (12) through the contact holes (17) and (18).

In the production method for an liquid crystal display device in this example, a line beam L0, having laser beam irradiation areas elongated in the X direction and a half width in a laser beam intensity profile in the Y direction narrower than the pixel spacing in the Y direction, irradiates the projected formation areas A1 of the TFT (10) for pixels arranged in the X direction in this way in a laser annealing treatment. Specifically, irradiating such a line beam while overlapping can increase evenness by making the period of the crystallinity of the polysilicon less than the pixel spacing. Restricting the laser irradiation areas to just the areas where TFT will be fabricated can also improve throughout. /13

In this example, when continuously melt-crystallizing the silicon film (30) while moving the substrate (20) and the line beam L0 relative to each other in the Y direction, the stage (40) is moved at low speed when the line beam L0 irradiates the projected formation areas A1 or A2 of the TFT (10) or the data driver part (7), and the stage (40) is moved at high speed when the line beam L0 irradiates other areas as shown in Figs. 8(A) and 8(B). Being thus able to reduce the time spent irradiating the laser on unnecessary areas can shorten annealing time and improve throughput.

Although the TFT (10) in the active matrix part (9) form a linear array in the X direction, the TFT (10) in the data driver part (7) do not form a linear array. In this example, laser annealing treatment is applied to all of the areas matching the data driver part (7). As a result, because the TFT (10) of the data driver part (7) can be fabricated from a polycrystalline silicon film (30), the TFT (10) of the data driver part (7) have high mobility. The laser annealing treatment of this example can be employed when an active matrix substrate has a data driver part or a partial data driver

part.

The channel area (13) of the TFT (10) is set so that the channel length direction is the X direction, which matches the longitudinal direction of the line beam. This inhibits an inadequately annealed part occurring from the source area (11) to the drain area (12) in the channel area (13). As a result, this stabilizes the electrical characteristics of the TFT (10). This also has the advantage that the alignment precision in the channel length direction during the patterning step can be relaxed when the patterning step is applied after the laser annealing step.

Applying the patterning step after the laser annealing step also means that a laser beam does not directly irradiate the underlayer protective film (21). Therefore, this can prevent damaging the underlayer protective film (21). Because the hue of the silicon film /14
(30) after the laser annealing treatment differs depending on the degree of irradiation of the laser beam, this difference in hue can identify the anneal pattern of the laser annealing treatment. As a result, there is no obstruction to aligning the anneal pattern of the laser annealing treatment with the mask pattern used in the patterning step. Aligning in this way patterns following the actual anneal pattern, which produces high positioning precision. This high positioning precision can also improve throughput even more when applying a production method in which a line beam having a long laser beam irradiation area in the Y direction irradiates the channel areas (13), which are arrayed in the Y direction in this example, and only the channel areas are annealed.

## BRIEF EXPLANATION OF THE DRAWINGS

Fig. 1(A) is a schematic diagram illustrating the configuration of an active matrix substrate in a liquid crystal display device according to a working example of the present invention, and Fig. 1(B) is a diagram illustrating a CMOS circuit used as the drive circuit of this device. Fig. 2 is an enlarged plan showing a pixel area on a active matrix substrate. Fig. 3(A) is a section of Fig. 2 taken at line I-I', and Fig. 3(B) is a section of Fig. 2 taken at line II-II'. Fig. 4 is a TFT step section corresponding to the section of Fig. 2 taken at line I-I'. Fig. 5 is a TFT step section corresponding to the section of Fig. 2 taken at line II-II'. Fig. 6 is a schematic diagram illustrating parts of a silicon film which require annealing. Fig. 7(A) is a schematic diagram illustrating how a laser beam is irradiated in the annealing step in Working Example 1 of the present invention, Fig. 7(B) is an intensity profile of this laser beam in the Y direction, and Fig. 7(C) is an intensity profile of another laser beam in the Y direction. Fig. 8(A) is a schematic

diagram illustrating how a laser beam is selectively irradiated in the annealing step in Working Example 1 of the present invention, and Fig. 8(B) is a diagram illustrating the movement speed of the substrate during this irradiation. Fig. 9 is a schematic diagram illustrating how patterning is applied after the annealing step in Working Example 1 of the present invention. Fig. 10 is a TFT step section corresponding to the section of Fig. 2 taken at line II–II' in Working Example 2 of the present invention. Fig. 11 is a TFT step section corresponding to the section of Fig. 2 taken at line II–II" in Working Example 2 of the present invention. Fig. 12 is a schematic diagram illustrating how a laser beam is irradiated in the annealing step in Working Example 2 of the present invention. Fig. 13(A) is a /15
schematic diagram illustrating how a laser beam is selectively irradiated in the annealing step in Working Example 2 of the present invention, and Fig. 13(B) is a diagram illustrating the movement speed of the substrate during this irradiation. Fig. 14 is a schematic diagram illustrating how a laser beam is selectively irradiated in the annealing step in Working Example 3 of the present invention. Fig. 15 is a schematic diagram illustrating how an alignment pattern is formed using laser beam irradiation in the annealing step in Working Example 4 of the present invention. Fig. 16 is a schematic diagram illustrating an alignment mark formed on the underlayer protective film in Working Example 5 of the present invention. Figs. 17(A) to (C) are diagrams illustrating the positional relationship between laser beam irradiation areas and areas irradiated by an arc lamp for rapid thermal annealing in Working Example 6 of the present invention.

EXPLANATION OF REFERENCE NUMERALS

1 … liquid crystal display device
2 … active matrix substrate
3 … data line
4 … scanning line
5 … pixel area
6 … liquid crystal capacitor
7 … data driver part
8 … scan driver part
9 … active matrix part
10 … TFT
11 … source area
12 … drain area
13 … channel area
14 … gate insulating film
15 … gate electrode
50 … optical system with a spot-shaped line beam
60 … photocuring resin for forming an alignment pattern